**Next Semester Plans for the Low Power, Low Noise CMOS Biosensor Chip Project:**

Since we have been working on the characterization process, we should be able to decide what speed, VDD, and process we will use for our project. This will give us the opportunity of designing our circuits using a specific model using a specific VDD, rather than doing a sweep or doing multiple simulations for all four processes.

![Figure 1: System Schematic](image)

What we plan on doing next semester is to design all the individual parts in Figure 1 in conjunction with the graduate students on our team. Matt will be finishing up the multiplier over break and then we will both be working together to design the low noise amplifier during the course of next semester. We will have to look at various design techniques to achieve a low enough noise figure given our power constraints (typically noise can be decreased by increasing the current in the transistor, but our design will have to employ other methods). We will also have to learn how to use the layout tools in Cadence to get a physical layout ready for device fabrication. We plan on finishing the design of each part of Figure 1, except the Wireless or USB, by the end of the next semester.