Next Year Plans for the Low Power, Low Noise CMOS Chip Design Project:

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There is certainly a lot of good work that can still be done on this project. The chip is really in its infancy when you look at how far we still have to go to get a fully functional prototype going. While we were able to accomplish a lot this semester in terms of process characterization and design of some of the core components of the chip, there is still a lot to be done in terms of detailed design.

From a digital perspective, future senior design students could look at how our 32-bit adder and 32-bit multiplier could be used to create more complicated signal processing blocks, like a fast fourier transform circuit for example. The DSP is still somewhat of a black box so there is plenty of work that could be done to figure out what goes inside of it.

On the other side, from an analog perspective there is also much work to be done. There is still a need for an initial design of a low noise pre amplifier and main amplifier to convert the analog electrode currents into digital signals. Also, a potentiostat needs to be designed which is basically an op amp that maintains the electrode at a constant reference potential, which is essential to getting good current measurements. There is also a need for an A/D converter. This would have to be a low-speed, high resolution converter that would be the bridge between the analog current and the digital signals. Finally, it would be useful to look into switched capacitors as another alternative voltage regulator topology, as the current one only has an efficiency of 48%.