CMOS 65nm Process Monitor

Advisors: Dr. Hugh Grinolds
Mr. Brian Misek
What is Process Variation?

The process parameters can vary from:
• Lot-to-Lot (interprocess variation)
• Wafer-to-wafer (interprocess variation)
• Die-to-die (intraprocess)

Variations in process parameters include:
• Doping densities
• Oxide thickness
• Diffusion depths
• W and L of transistors

These variations are strongly correlated so it’s difficult to isolate individual parameters
Die-to-Die Variation

I_{dsat} NMOS vs. I_{dsat} PMOS graph with data points indicating SF, FF, SS, and FS. The graph shows variations in the devices' characteristics.

Spec, SkewTarget, and W1 markers are used to denote specific performance targets and data sets.

Courtesy: Brian Misek
Variations on a Wafer

Frequency

- Fast
- Failed
- Slow
- Mid

A* 89 57.79%
B* 2 1.30%
Z* 11 7.14%
Y* 52 33.77%
Layout (Cadence)

NAND
Our Process Monitor

- On-die
- 65nm process compatible

Selector Block -> Inverter Delay Module

Poly Resistance Module

Future Expansion

Output Register
Our Design Constraints

Requirements:
• Size: < 100um x 100um per module
• Power-down mode
• Digital Output → one 8-bit word

Provided:
• 62 – 312 MHz Precision clock
• 1V supply
• Access to off-chip memory
The Inverter Delay Module consists of several components:

1. **Control Logic (On/Off)**
2. **Ring Oscillator Approx. 50-100 stages**
3. **Fast Counter Block**
4. **Processing Block**
5. **Output Digital Circuit**
Main Test Structure: Ring Oscillator

- Simple (can be designed with INV, NAND, or NOR)
- Large number of stages in a RO provide statistical normalization
- Frequency easily measured with counters
- Importance of propagation delay
  - Minimize power consumption in digital circuits
  - Provides a reference point for measuring other parameters
Ring Oscillator Operation

\[ f_{RO} = \frac{1}{N(t_{PLH} + t_{PHL})} \]

- RO has odd \( N \) stages
- Process variations affect delay time of each stage, reflecting frequency shifts in the freq. domain
Counter

Fast Counter
• 3-input NAND-NAND logic
• Minimal stages
• Small size transistors
Polyresistance Module

- Use two different test structures
- Resistively loaded ring oscillator
- Second test structure still in research phase
  - Non-linear oscillator
  - PTAT driven structure
RO Test Structure - Resistance

- Control Logic (On/Off)
- Resistively Loaded Ring Oscillator
- Fast Counter Block
- Inverter Delay Module
- Processing Block
- Output Digital Circuit
Resistively Loaded RO

At 2KΩ, \(\Delta R = 7\% \rightarrow \Delta f = .5\%\)
$f$ vs. $R$ (Corner Simulation)
Timeline

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We have no expected expenditures for next semester
Thank You

- Mr. Brian Misek
- Avago Technologies
- Dr. Hugh Grinolds
- Charles Thangaraj
Wafer-to-Wafer Variation

Selected Die from Skew

\[ I_{dsat} \]

Spec

SkewTarget

W1

W3

W4

W5

W6

W7

W8

W9

W10

Courtesy: Brian Misek
Process Geometry Rules

- N+ or P+ dimensions equal island dimensions.

**Layout Sheet for 65nm**

65nm is integral dimension.

- Well contacts must have N+ or P+
- N+ and P+ coincident with island
- Poly-to-contact not allowed.
- M2-to-island must have M1
- M2-to-poly must have M1

Provided by Dr. Hugh Grinolds
Next Steps

- Finish 2\textsuperscript{nd} test structure for resistance module
- Finish control logic
- Layout
- Documentation
- Preliminary work on threshold voltage module