In parallel mode, we can use LDC0 (not required). LDC0 is a user I/O after boot, so using LDC0 with parallel flash allows for using the flash after boot. DONE is a dedicated output and stays high after configuration, permanently disabling the flash.

**Slave-Parallel mode:**
- M[0:2] = 1 1 0
- S3: Position 2-1 (pull down CCLK_IN to the PROM)
- R144-R150 = install
- S1=4 = ON
- Pulldown CSI_B and RDWR_B on FPGA

**Serial mode:**
- M[0:2] = 0 0 0
- R144-R150 = remove (not needed, no harm in leaving them connected though)

Master BPI will work as well with same configuration as parallel, but requires far more I/Os on the FPGA (46)
- M[0:2] = 0 1 1
Primary bias control is through the opamp controlling the feedback. This is a bit finicky based on op-amp feedback and requires compensation to keep stability. The feedback approach requires 30ms for the LDO to stabilize after enabling.

Place the transistor approach in as an alternate option in case the feedback approach is too unstable in application.
For the Zetex current sense ICs:

Iout = 0.1 * Isense
Vout = Iout * Rout

Vout = 0.1 * Isense * Rout
If VCC_JTAG == VCCAUX, then no current limit resistors are required. If they are different, then current limit resistors are required.

VCCO_2 contains the configuration interface, and must match VCCO_FLASH. If VCCO2 is not the same as VCCAUX, then consult Xilinx App. Notes on current limiting.

VCCO_1

Jtag Voltage Select, default to 2.5V (Vccaux)

VCC_1.8V

VCC_2.5V

VCC_3.3V

VCCAUX

VCC_2.5V

VCC_3.3V

3.3V_DIG

VCC_Flash

VCC_3.3V

VCCO_1

VCCO_0

If VCCO_2 is not the same as VCCAUX, then consult Xilinx App. Notes on current limiting.
Filtering based on Xilinx appnote XAPP923.
Bias Must be a net > 3V, lower is better for efficiency

Adjust Vout for right above the dropout of the 5V_A LDO (5.35V). Note: PC104 max voltage is 5.25V, so this is technically out of spec. The TS7300 has wide range of Vin for its regulators, so that's not a problem, but if another card is plugged into the PC104 bus, then make sure it's capable of handling 5.4V

TODO: Change 16.2K to 20K
Note: Jumpers must be placed on unused RTD header connectors

Provides reference plus minimum
common mode voltage

ADC output = Rrtd/Ref * 2^N
The 200-ohm resistors are current-limit resistors in case a 5V source drives the lines. The TS7300 is 3.3V, but is compatible with 5V devices.

BHE is used as bus-high enable to enable 16-bit xfr, normally on the second PC104 connector.
If there's room, add in a Parallel-3 type JTAG header (6 pin .1 pitch).