An Outlier Detection Based Approach for PCB Testing

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Abstract

Agilent’s Capacitive Lead Frame Testing technique (a.k.a. “Test Jet or ‘VTEP’”) for printed circuit boards is based on measurement of capacitance between a plate placed above vacant connectors on a PCB and the individual pins/nets accessed via a bed of nails fixture. Faults such as opens and shorts manifest as different capacitance values. As the circuit boards and connectors become dense, the threshold based techniques for detection of capacitance values fail. Furthermore, automated procedures are required to scale the test method and overcome board-to-board and fixture-to-fixture variations that are present.

We are developing an outlier detection scheme for automatically detecting faulty boards and connectors. The scheme, based on Principal Components Analysis (PCA), treats the capacitance measurement set of a board in a holistic manner to overcome the above limitations. The set of measurements for each board is converted to a distance (d) with respect to all the boards, and the outliers can be detected based on this distance. The method is validated using test data on DDR3 (RAM) connector/boards measurements carried out on Agilent 3070 testers. The outliers can be observed on the right side of the CDF plot of the d(t) values. Ongoing work is aimed at further evaluation of the technique and refining it to increase the sensitivity of the method.

Capacitive Lead Frame Testing Device

The pin under test is connected to an AC signal source; all other pins are connected to the ground.

Suspended on the top of the tested connector, the sense plate forms a capacitive path from the tested pin. An open defect on the signal pin decreases the capacitance.


PCA Based Outlier Detection --- Algorithm

Obtain measurement matrix $M \ (m \times n \ test \ pins)$.

Center matrix $M$ by subtracting average value of each pin column.

Calculate $Z_{mn}$ matrix of Z score (Principal Components):

$Z_{mn} = \frac{M - \mu}{\sigma}$

where $M$ is the measured data, $\mu$ is the mean value, and $\sigma$ is the standard deviation.

Find the Z score value of boards with matrix $Z = m \times n$.

$Z_{mn}$: scaled version of PC scores

The z-score values are squared; diagonal values are eigenvalues arranged in ascending order.

$Z_{mn}$: rows contain eigen vectors.

Calculate D1 value for each board:

$d_1^2 = \sum_{k=1}^{p} z^2_{ik}$

where $d_1^2$ is the D1 value, $p$ is the number of PCs that contribute to D1 value,

$z_{ik}$ is the Z score of the k_th PC for the i_th board.

Sort boards according to $d_1^2$; Plot the cumulative distribution of $d_1^2$ values; Outliers appear on the right side.

PCA Based Outlier Detection --- Results

- The outliers stand out at the high-end of the $d_1$ scale.
- (Ex.: 17,18,19,20,21,22 are clear outliers. 5, 4, 14,15 are possible outliers)

Localized Analysis Based on Pin Configuration of Connector

- Localized Analysis based on pin configuration of connector
- The 240 connector pins are divided into 10 test windows and the analysis is performed on each window.

Localized Analysis Based on Pin Configuration of Connector

- As a fault in a pin is likely to affect only the neighboring pins, analysis of localized clusters of pins may provide better sensitivity.
- The 240 connector pins are divided into 10 test windows and the analysis is performed on each window.

Test Window Analysis

- Test windows 9, 10, corresponding to pins at the right end of J24 connector, contain outliers.
- The method is more capable of detecting outliers based on localized values. For example, window 9 identifies boards 11 as possible outliers while they were not detected when analysis was performed on the full data set.

Summary and Future Work

- An outlier detection scheme was presented for identifying faults in pins of PCBs. The Principal Components Analysis based technique enhances the test process by allowing for automation of faulty board and pin identification.
- The outlier related information is extracted by this PCA into a single D value, which allows the identification of potential defect devices. By performing the analysis on small windows of pins, the sensitivity of the scheme can be further improved.
- Sensitivity of the scheme to measurement tolerances, etc. is being investigated as well as use of different distance measures for fault detection.
- We are investigating techniques to enhance the efficiency of outlier detection related computations for on-line testing. Also under investigation are techniques to diagnose faults based on cumulative experience with different circuit boards.

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